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10/542,433	07/14/2005	Aaron Reel Bouillet	PU030032	2767

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EXAMINER	
CHAI, LONGBIT	
ART UNIT	PAPER NUMBER
2431	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/542,433	BOUILLET, AARON REEL	
	Examiner	Art Unit	
	LONGBIT CHAI	2431	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/27/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant's claim for benefit of foreign priority under 35 U.S.C. 119 (a) – (d) is acknowledged.

The application is a 371 case of PCT/US04/01581 application filed on 4/12/2005 and has a foreign priority application filed on 1/17/2003.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 3, 9 – 11 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Oh (U.S. Patent 2001/0048723).

As per claim 1, Oh teaches a signal processing apparatus comprising:

a source of a fixed rate digital signal (Oh: Para [0008] Line 4 – 5: a A/D conversion clock is a fixed rate clock, which is different from a symbol clock);

a signal processor operating in a synchronous-sampling mode for producing a control signal representing a symbol rate (Oh: Para [0011], Para [0024] and Para [0023] Line 3 – 5: (a) a synchronous-sampling mode is an operating mode where a A/D converter

takes samples coincident with the digital symbol locations, and (b) Oh teaches a steady symbol timing (i.e. a symbol rate) is restored at the A/D signal processor by synchronizing the A/D conversion clock (i.e. fixed-rate clock) with a symbol clock wherein a symbol is extracted (i.e. is sampled – to yield samples) in the original symbol location by interpolating the digital signal converted in the A/D conversion step, in accordance with the control of the timing processor (i.e. a control signal), and outputs a digital signal in which timing is restored (i.e. symbol timing / rate) and as such a carrier wave can be restored by correcting frequency and phase distortions of the symbol, which is extracted in the extracting step in accordance with a clock in which symbol timing / clock is restored); and

an interpolator responsive to the control signal for processing the fixed rate digital signal to yield samples at the symbol rate (see the same rationale as above).

As per claim 9, Oh teaches a method of signal processing comprising the steps of:

receiving a plurality of digital values at a fixed rate of time (Oh: Para [0008] Line 4 – 5: a A/D conversion clock is used as a fixed rate clock, which is different from a symbol clock, to produce a plurality of digital values at a fixed rate of time);

receiving a control signal from a signal processor operating in a synchronous-sampling mode (Oh: Para [0011] and Para [0024] and Para [0023] Line 3 – 5: (a) a synchronous-sampling mode is an operating mode where a A/D converter takes samples coincident with the digital symbol locations, and (b) Oh teaches a steady symbol timing (i.e. a symbol rate) is restored at the A/D signal processor by synchronizing the A/D conversion clock (i.e. fixed-rate clock) with a symbol clock wherein a symbol is extracted (i.e. is sampled – to yield samples) in the original symbol location by interpolating the digital signal converted in the A/D conversion step, in accordance with the control of the timing processor (i.e. a control

signal), and outputs a digital signal in which timing is restored (i.e. symbol timing / rate) and as such a carrier wave can be restored by correcting frequency and phase distortions of the symbol, which is extracted in the extracting step in accordance with a clock in which symbol timing / clock is restored); and

calculating a signal level by interpolating the signal level from the plurality of digital values (Oh: Para [0023] Line 3 – 5, Para [0011] and Para [0024]: the timing processor (i.e. w.r.t. the control signal) calculates timing errors to restore timing and, as a result, generates / calculate a plurality of location signal levels which indicate the optimal symbol locations).

As per claim 15, Oh teaches a signal processing apparatus comprising:

a source of an analog signal (Oh: Para [0008] Line 4 – 5: a A/D signal processor has a source of an analog signal);

an analog to digital converter for converting the analog signal to a fixed rate digital signal (Oh: Para [0008] Line 4 – 5: a A/D conversion clock is used as a fixed rate clock, which is different from a symbol clock, to produce a plurality of digital values at a fixed rate of time);

a demodulator operating in a synchronous-sampling mode (Oh: Figure 1 / Element 16, Para [0011], Para [0024] and Para [0023] Line 3 – 5: (a) a Matched Filter is a demodulator and a synchronous-sampling mode is an operating mode where a A/D converter takes samples coincident with the digital symbol locations, and (b) Oh teaches a steady symbol timing (i.e. a symbol rate) is restored at the A/D signal processor by synchronizing the A/D conversion clock (i.e. fixed-rate clock) with a symbol clock wherein a symbol is extracted (i.e. is sampled – to yield samples) in the original symbol location by interpolating the digital signal converted in the A/D conversion step, in accordance with the control of the timing processor (i.e. a control

signal), and outputs a digital signal in which timing is restored (i.e. symbol timing / rate) and as such a carrier wave can be restored by correcting frequency and phase distortions of the symbol, which is extracted in the extracting step in accordance with a clock in which symbol timing / clock is restored);

a processor for producing a control signal representing a symbol rate (see the same rationale as above); and

an interpolator responsive to the control signal for processing the fixed rate digital signal to yield samples at the symbol rate by calculating a symbol value at a symbol location by interpolating a number of fixed rate samples adjacent to said symbol location and outputting the samples to the demodulator (Oh: Figure 2 & Para [0023] Line 3 – 5, Para [0011] and Para [0024]: an interpolator responsive to the timing processor (i.e. w.r.t. the control signal) calculates timing errors to restore timing and, as a result, generates / calculate a plurality of location signal levels which indicate the optimal symbol locations and as such a carrier wave can be restored by correcting frequency and phase distortions of the symbol, which is extracted in the extracting step in accordance with a clock in which symbol timing / clock is restored).

As per claim 2, Oh teaches the interpolator processes the fixed rate digital signal to yield samples at the symbol rate by calculating a symbol value at a symbol location by interpolating a number of fixed rate samples adjacent to the symbol location (Oh: Para [0011] and Para [0024], Para [0023] Line 3 – 5 and Para [0023] Line 3 – 5: (a) a synchronous-sampling mode is an operating mode where a A/D converter takes samples coincident with the digital symbol locations, and (b) Oh teaches a steady symbol timing (i.e. a symbol rate) is restored at the A/D signal processor by synchronizing the A/D conversion clock (i.e. fixed-rate clock) with a symbol

clock wherein a symbol is extracted (i.e. is sampled – to yield samples) in the original symbol location by interpolating the digital signal converted in the A/D conversion step, in accordance with the control of the timing processor (i.e. a control signal), and outputs a digital signal in which timing is restored (i.e. symbol timing / rate) and as such a carrier wave can be restored by correcting frequency and phase distortions of the symbol, which is extracted in the extracting step in accordance with a clock in which symbol timing / clock is restored and (c) the timing processor (i.e. w.r.t. the control signal) calculates timing errors to restore timing and, as a result, generates / calculate a plurality of location signal levels which indicate the optimal symbol locations).

As per claim 3 and 11, Oh teaches the source of the fixed rate digital signal is an analog to digital converter (Oh: Para [0008] Line 4 – 5: a A/D conversion clock is used as a fixed rate clock, which is different from a symbol clock, to produce a plurality of digital values at a fixed rate of time).

As per claim 10, Oh teaches the control signal from the signal processor is a symbol rate ((Oh: Para [0011], Para [0024] and Para [0023] Line 3 – 5: (a) a synchronous-sampling mode is an operating mode where a A/D converter takes samples coincident with the digital symbol locations, and (b) Oh teaches a steady symbol timing (i.e. a symbol rate) is restored at the A/D signal processor by synchronizing the A/D conversion clock (i.e. fixed-rate clock) with a symbol clock wherein a symbol is extracted (i.e. is sampled – to yield samples) in the original symbol location by interpolating the digital signal converted in the A/D conversion step, in accordance with the control of the timing processor (i.e. a control signal), and outputs a digital signal in which timing is restored (i.e. symbol timing / rate) and as such a carrier wave can be restored by

correcting frequency and phase distortions of the symbol, which is extracted in the extracting step in accordance with a clock in which symbol timing / clock is restored)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4, 5, 7, 8, 12 13, 16, 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh (U.S. Patent 2001/0048723), in view of MacLean et al. (U.S. Patent 2002/0110376).

As per claim 4, 12 and 16, Oh does not disclose expressly the interpolator is a cubic interpolator.

MacLean teaches the interpolator is a cubic interpolator (MacLean: Para [0136]).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of MacLean within the system of Oh because (a) Oh teaches an interpolator responsive to the timing processor (i.e. w.r.t. the control signal) calculates timing errors to restore timing and, as a result, generates / calculate a plurality of location signal levels which indicate the optimal symbol locations (Oh: Figure 2 & Para [0023] Line 3 – 5, Para [0011] and Para [0024]), and (b) MacLean teaches a interpolator can be design as a cubic interpolator (MacLean: Para [0136]).

As per claim 5, 13 and 17, Oh does not disclose expressly the interpolator is a linear interpolator.

MacLean teaches the interpolator is a linear interpolator (MacLean: Para [0136]).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of MacLean within the system of Oh because (a) Oh teaches an interpolator responsive to the timing processor (i.e. w.r.t. the control signal) calculates timing errors to restore timing and, as a result, generates / calculate a plurality of location signal levels which indicate the optimal symbol locations (Oh: Figure 2 & Para [0023] Line 3 – 5, Para [0011] and Para [0024]), and (b) MacLean teaches a interpolator can be design as a linear interpolator (MacLean: Para [0136]).

As per claim 7 and 19, Oh does not disclose expressly the interpolator is internal to an integrated circuit.

MacLean teaches the interpolator is internal to an integrated circuit (MacLean: Para [0123] and [0122]).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of MacLean within the system of Oh because (a) Oh teaches an interpolator responsive to the timing processor (i.e. w.r.t. the control signal) calculates timing errors to restore timing and, as a result, generates / calculate a plurality of location signal levels which indicate the optimal symbol locations (Oh: Figure 2 & Para [0023] Line 3 – 5, Para [0011] and Para [0024]), and (b) MacLean teaches the interpolator is internal to an integrated circuit (MacLean: Para [0123] and [0122]).

As per claim 8 and 20, Oh does not disclose expressly the interpolator is implemented using software.

MacLean teaches the interpolator is implemented using software (MacLean: Para [0123] and [0122]).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of MacLean within the system of Oh because (a) Oh teaches an interpolator responsive to the timing processor (i.e. w.r.t. the control signal) calculates timing errors to restore timing and, as a result, generates / calculate a plurality of location signal levels which indicate the optimal symbol locations (Oh: Figure 2 & Para [0023] Line 3 – 5, Para [0011] and Para [0024]), and (b) MacLean teaches the interpolator is implemented using software (MacLean: Para [0123] and [0122]).

4. Claims 6, 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh (U.S. Patent 2001/0048723), in view of Knutson et al. (U.S. Patent 5,878,088).

As per claim 6, 14 and 18, Oh does not disclose expressly the interpolator is a piecewise parabolic interpolator.

Knutson teaches the interpolator is a piecewise parabolic interpolator (Knutson: Column 7 Line 1 – 6).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Knutson within the system of Oh because (a) Oh teaches an interpolator responsive to the timing processor (i.e. w.r.t. the control signal) calculates timing errors to restore timing and, as a result, generates / calculate a plurality of location signal levels which indicate the optimal symbol locations (Oh: Figure 2 & Para [0023]

Line 3 – 5, Para [0011] and Para [0024]), and (b) Knutson teaches a interpolator can be design as a piecewise parabolic interpolator (Knutson: Column 7 Line 1 – 6).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LONGBIT CHAI whose telephone number is (571)272-3788. The examiner can normally be reached on Monday-Friday 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y. Vu can be reached on 571-272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Longbit Chai/

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09/30/2008